

### In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 27 (Cancelled)

28. (Currently Amended) ~~The A~~ data processing apparatus ~~of~~  
~~claim 25, further comprising:~~

a first multiply circuit having first and second inputs and an output, said first multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a first product at said output;

a first Q shifter having an input receiving said first product from said first multiply circuit and an output ~~supplying said first input to said adder/subtractor circuit~~, said first Q shifter shifting said first product an instruction specified number of bits responsive to the rounding dot product instruction; ~~and~~

a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output;

a second Q shifter having an input receiving said second product from said second multiply circuit and an output ~~supplying said second input to said adder/subtractor circuit~~, said second Q shifter shifting said second product said instruction specified number of bits responsive to the rounding dot product instruction;

an adder/subtractor circuit having first and second inputs, a mid-position carry input to a predetermined bit and an output, said first input receiving said shifted first product from first Q shifter, said second input receiving said shifted second product from said second Q shifter, said adder/subtractor circuit operable in response to said dot product instruction to arithmetically

27 combine said first and second products and a "1" input at said  
28 mid-position carry input of said predetermined bit thereby forming  
29 a mid-position rounded sum; and  
30 a shifter connected to receive said mid-position rounded sum  
31 of the adder/subtractor circuit, the shifter operable to shift said  
32 mid-position rounded sum a predetermined amount in response to said  
33 dot product instruction.

1 29. (Currently Amended) ~~The A~~ data processing apparatus ~~of~~  
2 ~~claim 25, wherein comprising:~~

3 a first multiply circuit having first and second inputs and an  
4 output, said first multiply circuit operable in response to a dot  
5 product instruction to multiply data received at said first and  
6 second inputs and generate a first product at said output, said  
7 first multiply ~~generates~~ generating said first product in a  
8 redundant sign/magnitude format;

9 a second multiply circuit having first and second inputs and  
10 an output, said second multiply circuit operable in response to a  
11 dot product instruction to multiply data received at said first and  
12 second inputs and generate a second product at said output, said  
13 second multiply circuit ~~generates~~ generating said second product in  
14 said redundant sign/magnitude format;

15 an adder/subtractor circuit having first and second inputs, a  
16 mid-position carry input to a predetermined bit and an output, said  
17 first input receiving said first product from said first multiply  
18 circuit, said second input receiving said second product from said  
19 second multiply circuits, said adder/subtractor circuit operable in  
20 response to said dot product instruction to arithmetically combine  
21 said first and second products and a "1" input at said mid-position  
22 carry input of said predetermined bit thereby forming a  
23 mid-position rounded sum, said adder/subtractor circuit  
24 arithmetically ~~combines~~ combining said first and second products

25 and said "1" input at said mid-position carry input forming said  
26 mid-position rounded sum in said redundant sign/magnitude format;  
27 a shifter connected to receive said mid-position rounded sum  
28 of the adder/subtractor circuit, the shifter operable to shift said  
29 mid-position rounded sum a predetermined amount in response to said  
30 dot product instruction, said shifter ~~shifts~~ shifting said  
31 mid-position rounded sum in said redundant sign/magnitude format;  
32 and  
33 ~~said data processing apparatus further comprises~~ a carry save  
34 adder to 2's complement converter having an input receiving said  
35 shifted mid-position rounded sum in said redundant sign/magnitude  
36 format from said shifter and an output generating a corresponding  
37 normal coded format.